ABSTRACT

The invention allows the execution of a PC relative branch instruction with displacement is speeded up without changing the instruction operations of existing processors and without requiring new instructions. The branch target address calculation is made faster by calculating the lower portion of the branch target address prior to storing the instruction word in a cache or buffer, and writing the calculation result into the displacement field of the instruction word and into a bit that has been added to the cache or the buffer, such that some calculation is executed simultaneously to be skipped later at the time of execution of the instruction by using the executed calculation result stored in the cache or buffer.